CLAIMS

What is claimed is:

1. A method of forming a nanotube memory cell on a semiconductor substrate, the method comprising:

forming a first silicon filled chamber overlying a first and second contact formed in the substrate;

forming a nanotube layer on the first silicon filled chamber, the nanotube layer overlying the first contact and not overlying a second portion of the first silicon filled chamber, the second portion overlying the second contact;

forming a second silicon filled chamber directly on the nanotube layer;

forming a dielectric layer on the second silicon filled chamber;

patterning the dielectric layer to form an access contact hole exposing the second silicon filled chamber, the contact hole formed to overly the second portion of the first chamber;

etching the first and second silicon filled chambers using the contact hole to remove the silicon; and

depositing a conductive material on the dielectric layer such that the conductive material makes contact with the second contact and closes the aperture created by the contact hole.

2. The method as recited in claim 1, wherein the dielectric layer is a nitride layer.

3. The method as recited in claim 1, wherein forming the first silicon filled chamber comprises depositing a nitride layer on the substrate and patterning and etching the nitride layer to form a trench overlying the first and second contacts.

4. The method as recited in claim 1, wherein forming the second silicon filled chamber comprises depositing an oxide layer on the nanotube layer and patterning and etching the oxide layer to form a trench overlying the first and second contacts.

5. The method as recited in claim 1, wherein the contact hole is positioned over the second contact.

6. The method as recited in claim 1, wherein the second contact is located a predetermined distance from the first contact, the predetermined distance being a function of the flow properties of the conductive material selected for filling the contact hole.

7. The method as recited in claim 1, wherein the first and second contacts provide electrical contact with a first and second diffusion area on the substrate.

8. The method as recited in claim 1, wherein patterning the dielectric layer further comprises exposing the nanotube layer and wherein depositing a conductive material on the dielectric layer further comprises making electrical contact between the exposed nanotube layer and the conductive metal.

9. The method as recited in claim 3, wherein the contact hole is formed to access the second trench at a location distal from the first contact.

10. The method as recited in claim 1, wherein etching the first and second silicon filled chambers is performed using N-methyl pyrrolidinone (NMP) as an etching solvent.

11. The method as recited in claim 1, further comprising patterning and etching the conductive layer to form an upper electrode and a contact electrically connected to the nanotube layer.

12. The method as recited in claim 1, wherein the first silicon filled chamber has a thickness in the range of 10 to 50 nm.

13. The method as recited in claim 1, wherein the second silicon filled chamber has a thickness in the range of 10 to 50 nm.

14. The method as recited in claim 1, wherein forming the first silicon filled chamber comprises depositing a nitride layer on the substrate and patterning and etching the nitride layer to form a trench overlying the first and second contacts and wherein forming the second silicon filled chamber comprises depositing an oxide layer on the nanotube layer and patterning and etching the oxide layer to form a trench overlying the first and second contacts.

15. The method as recited in claim 1, wherein the first silicon filled chamber is approximately the same size as the second silicon filled chamber.

16. A method of forming a nanotube memory cell on a semiconductor substrate, the method comprising:

forming a first trench overlying a first and second contact formed in a nitride layer;

filling the first trench with silicon to form a memory cell lower chamber;

forming a patterned nanotube layer over the memory cell lower chamber, the nanotube layer patterned such that the portion of the lower chamber overlying the second contact is exposed;

forming a second trench on the nanotube layer such that the second trench overlies the first and second contact;

filling the second trench with silicon to form a memory cell upper chamber;

depositing and patterning a nitride layer over the upper and lower chambers; to form an access opening to the nanotube layer and a second access opening to the second contact; and

depositing and patterning a conductive layer to form an upper electrode electrically connected to the second contact.

17. The method as recited in claim 16, wherein the first contact forms a bottom electrode of the memory cell.